Modified PTO/SB/33 (10-05)

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number	
Q77321	

Application Number	Filed
10/773,333	February 9, 2004
First Named Inventor	
Hiroshi OKUMURA	
Art Unit	Examiner
3663	Johannes P. MONDT

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Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal

The review is requested for the reasons(s) stated on the attached sheet(s).

☑ I am an attorney or agent of record.

Registration number 54,666

/ Andrew J. Taska /
Signature

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July 2, 2009
Date

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Docket No: Q77321
Hiroshi OKUMURA	
Appln. No.: 10/773,333	Group Art Unit: 3663
Confirmation No.: 8920	Examiner: Johannes P. MONDT
Filed: February 9, 2004	

For: THIN FILM TRANSISTOR SUBSTRATE AND METHOD OF MANUFACTURING THE SAME

PRE-APPEAL BRIEF REQUEST FOR REVIEW

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Sir:

Pursuant to the Pre-Appeal Brief Conference Pilot Program, and further to the Examiner's Final Office Action dated March 3, 2009, Applicant files this Pre-Appeal Brief Request for Review. This Request is also accompanied by the filing of a Notice of Appeal.

Under 35 U.S.C. § 103(a), claims 29, 16 and 34-36 are rejected as allegedly being unpatentable over Prior Art as Admitted by Applicant (hereinafter "APA"), Nakamura (JP 2003-017502A) and Adler (5,757,050); claim 14 is rejected over APA, Nakamura, Adler, and Zhang al. (6,507,069); claim 30 is rejected over APA, Nakamura, Adler, and Izawa et al. (5,053,849); claims 31 and 32 are rejected over APA, Nakamura, Adler, and Numasawa et al. (6,048,795); claim 33 is rejected over APA, Nakamura, Adler, and Suzawa et al. (5,914,498).

There are clear errors in all of the Examiner's rejections *at least* because the cited references fail to teach or suggest the features of "wherein said second active layer comprises a first channel region disposed

directly below said second gate electrode, a second channel region disposed directly below said third gate electrode and an impurity doping region disposed between said first and second channel regions such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode," as recited in independent claim 29. The Examiner acknowledges that APA fails to teach or suggest these features but, nevertheless, alleges that the region marked P:5E19/cm^3 on the right side of Nakamura's Drawing 4A, or alternatively a sub-portion of the darkened region marked P:4E17/cm^3, correspond to the recited "first channel region" and, thus, remedy the deficient teachings of APA. The clear errors in the Examiner's rejections are explained in detail below.

First, during the interview conducted on June 9, 2009, the Examiner conceded that his allegations that Nakamura's region marked P:5E19/cm^3 corresponds to the claimed "channel region" were in error. Nevertheless, the Examiner maintained that the region marked P:4E17/cm^3 in Nakamura still reads on the claimed "channel region." However, the Examiner's position relies on the conclusory allegation that there is nothing in the inherent properties of an LDD, or any other impurity doping region contiguous with a region that is at least during the ON state electrically connecting the source and the drain, that precludes it from functioning as a channel region. Accordingly, the Examiner interprets the "channel region" of claim 29 to require little more than an electron path between a source and a drain.

The Examiner's allegations in this regard are unsupported. The Examiner is required to give the claims their broadest reasonable interpretation (*see* MPEP §2111.01). One of ordinary skill in the art would not reasonably interpret the claimed "channel region" to include any impurity doping region contiguous with a region that is at least during the ON state, as alleged by the Examiner. The term "channel region" has a plain meaning to those of ordinary skill in the art that is clearly distinguishable from a lightly doped drain

region like that taught in Nakamura. Furthermore, contrary to the reasoning applied by the Examiner, one of ordinary skill in the art would have recognized that it is not necessary to use a transistor if it is always in an ON state. Thus, one of ordinary skill in the art would not have reasonably interpreted the claimed "channel region" to include Nakamura's lightly doped drain region marked P:4E17/cm^3.

Second, Nakamura itself distinguishes between a channel region (i.e., the region marked B:2E16/cm^3) and the lightly doped drain region marked P:4E17/cm^3 and, therefore, Nakamura expressly teaches away from the Examiner's proposed interpretation. For instance, as shown in Drawing 4A of Nakamura, the semiconductor layer consists of source and drain regions which are highly doped with n-type impurities (doped phosphorus (P) at a concentration of 5E19/cm^3 and these regions are referred to as "n^+ regions"). Nakamura's semiconductor layer also consists of LDD regions which are lightly doped with n-type impurities (doped phosphorus (P) at a concentration of 4E17/cm^3 and these regions are referred to as "n^- regions"). Moreover, Nakamura's semiconductor layer consists of a channel region which is slightly doped with p-type impurities (doped boron (B) at a concentration of 2E16/cm^3 and this region is referred to as a "p region" or an "i (intrinsic) region").

As demonstrated by the above description of Drawing 4A, Nakamura's channel region is completely different from the LDD regions. For example, the channel regions have different dopant conductive types and different doping concentrations than the LDD regions. Therefore, no one skilled in the art would reasonably take the position that any of such impurity doping regions corresponds to a "channel region," as claimed.

Third, the 06/15/09 Advisory Action alleges that Applicant's arguments are not persuasive simply because the amount of doping of Nakamura's LDD regions is closer to that of the central channel region

that it is to the conductivity of the source/drain regions. Applicant disagrees and submits that the Examiner has not provided any evidence in fact and/or reasoning in the official record to support such allegations. Moreover, even assuming *arguendo* that the Examiner's allegations that the magnitude of the conductivities stand in the ratio of channel : LDD : source/drain = 1 : 20 : 2,500 *were* supported, such a ratio alone fails to demonstrate that one of ordinary skill in the art would have reasonably interpreted a "channel region," as claimed, to include Nakamura's lightly doped drain region. Quite to the contrary, the Examiner's allegations actually support Applicant's position that Nakamura's channel region is completely different from the LDD regions disclosed therein since, if the Examiner's allegations *were* true, Nakamura would explicitly teach that the LDD regions therein exhibit completely different conductive properties than the channel region by a factor of 20 : 1 (i.e., several orders of magnitude).

Fourth, the Examiner's allegations that the relative horizontal extent of LDD doping regions, and particularly the feature of a non-overlapping portion of an LDD region, is an obvious matter of design choice because both with and without this feature, the performance of the TFT substrate is qualified as useful, are unsupported by Nakamura. Nakamura in no way demonstrates that the feature of a non-overlapping portion of an LDD region is an obvious matter of design choice. In contrast, Nakamura clearly discloses that the electric field produced near the boundary of a channel formation field and an LDD field is eased. To obtain this effect, Nakamura teaches that the electrode 17 should be overlapped with gate electrode 13 as shown in all plan views, particularly Drawing 1A. That is, Nakamura teaches that the electrode 17 should be arranged over the boundary of the channel formation field and an LDD field. Indeed, Drawing 4A of Nakamura is nothing more than a schematic model. Therefore, Nakamura does not

demonstrate that the feature of a non-overlapping portion of an LDD region is an obvious matter of design choice and cannot employ such a configuration.

In contrast to Nakamura, according to an illustrative embodiment shown in FIG. 11, the low voltage gate electrode 110 does not overlap LDD region 105f and the high voltage gate electrode 107 overlaps the LDD regions 105f and 105e. That is, the electric field is eased by a so-called LDD structure in the low voltage driving TFT including low voltage gate electrode 110 and a so-called GOLD structure in the high voltage driven TFT including high voltage gate electrode 107. Parasitic capacitance is more problematic in the low voltage driven TFT than in the high voltage driving TFT (*see* Specification, ¶25). Therefore, there can be formed a TFT substrate including a circuit which is constituted of plural kinds of TFTs with a high throughput and which can be driven at high speed with low power consumption. Furthermore, a sub-gate structure in the high voltage driving TFT is excellent in output controllability at a low gate voltage, and therefore, is appropriate for a high withstand voltage TFT used for a level shift circuit (*see* Specification, ¶35). Such a sub-gate structure would not have been obvious from APA in view of Nakamura.

In view of the above clear errors, claim 29 is patentable over the cited references for *at least* the above reasons and the dependent claims 14, 16 and 30-36 are patentable *at least* by virtue of their dependency. Accordingly, Applicant respectfully requests that these rejections be overturned.

Respectfully submitted,

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